IN THE CLAIMS:

Please cancel claims 2, 3, 17, 18, 22, and amend the claims as follows:

1. (Currently Amended) A synchronous memory system, comprising:

a plurality of memory modules in a main memory, with each memory module comprising at least two memory banks;

a memory control device configured to generate commands, wherein the commands comprise a plurality of command segments with a respective plurality of elements, wherein one of the command segments is a selection command segment for selecting at least two memory banks simultaneously, and wherein each of the memory banks has at least one uniquely associated element of the selection command segment; and

a transfer bus for communication between the memory control device and the plurality of memory modules, wherein the transfer bus is in the form of a daisy chain structure and wherein the transfer bus comprises a plurality of parallel transfer lines; and wherein the memory control device is configured to transfer the commands to the plurality of memory modules using the transfer bus, and wherein the transfer bus is configured to transfer the elements of a command segment in parallel over the parallel transfer lines, wherein the daisy chain structure comprises a first point-to-point connection from the memory control device to a first memory module of the plurality of memory modules and a second point-to-point connection from the first memory module of the plurality of memory modules to a second memory module of the plurality of memory modules, whereby the memory control device and the plurality of memory modules are interconnected to form a daisy chain, wherein each of the plurality of memory modules further comprises a buffer device, and wherein each buffer device is configured to determine whether an associated command needs to be forwarded to at least one of: (i) the at least two memory banks in the respective memory module; (ii) and the one or more other memory modules, based on the selection command segment.

2. (Cancelled)

3. (Cancelled)

4. (Currently Amended) The synchronous memory system of claim ~~2~~ 1, wherein the buffer device is configured to generate a chip select signal for the at least two memory banks.

5. (Original) The synchronous memory system of claim 1, where the selection command segment is the first segment of the commands.

6. (Original) The synchronous memory system of claim 1, wherein the number of transfer lines in the transfer bus is at least equal to the maximum number of memory banks which can be used in the memory system.

7. (Original) The synchronous memory system of claim 1, wherein the commands for each memory bank contain an element for a clock enable signal.

8. (Original) The synchronous memory system of claim 1, wherein the commands contain an element for a clock enable signal for all the memory banks.

9. (Original) The synchronous memory system of claim 1, wherein the commands for each memory bank contain an element for an on-die termination signal.

10. (Original) The synchronous memory system of claim 1, wherein the commands contain an element for an on-die termination signal for all the memory banks.

11. (Original) The synchronous memory system of claim 1, wherein the buffer device is designed to generate an on-die termination signal.

12. (Original) The synchronous memory system of claim 1, wherein the commands contain an element for a reset signal.

13. (Previously Presented) The synchronous memory system of claim 1, further comprising a transfer line connecting the memory control device and at least one of the plurality of memory modules and configured to propagate a reset signal.

14. (Original) The synchronous memory system of claim 1, wherein the commands contain an element for signaling that the command is intended for the buffer device.

15. (Previously Presented) The synchronous memory system of claim 1, wherein the memory control device comprises a coding device for coding generated commands and the buffer device comprises a decoding device for decoding received coded commands.

16. (Currently Amended) A method for communication, in a synchronous memory system, between a memory control device and a plurality of memory modules in a main memory using a transfer bus, where each of the plurality of memory modules comprises at least two memory banks, the method comprising:

generating, with the memory control device, commands comprising a respective plurality of command segments with a respective plurality of elements, wherein one of the command segments is a selection command segment for selecting at least two memory banks simultaneously, and wherein each of the memory banks has at least one uniquely associated element of the selection command segment; and

transmitting the commands to the plurality of memory modules using the transfer bus, with the plurality of elements being transferred in parallel over a plurality of parallel transfer lines of the transfer bus, wherein the transfer bus is in the form of a daisy chain structure and wherein the transfer bus comprises a first point-to-point connection from the memory control device to a first memory module of the plurality of memory modules and a second point-to-point connection from the first memory module of the plurality of memory modules to a second memory module of the plurality of memory modules, whereby the memory control device and the plurality of memory modules are interconnected to form a daisy chain;

receiving the commands from the transfer bus by a buffer device; and

determining whether a respective command needs to be forwarded to at least one of (i) the at least two memory banks in a respective memory module of the plurality of memory modules; and (ii) one or more other memory modules of the plurality of memory modules, based on the selection command segment.

17. (Cancelled)

18. (Cancelled)

19. (Currently Amended) The method of claim 16, further comprising:

~~receiving the commands from the transfer bus by a buffer device~~; and

~~comparing a bit pattern of the selection command segment with one or more predetermined bit patterns by the buffer device; and~~

upon determining~~, from the comparison,~~ that the selection command segment is destined for a memory bank associated with the buffer device~~;~~, ~~and~~

generating, by the buffer device, a chip select signal for the associated memory bank.

20. (Original) The method of claim 16, wherein the selection command segment is transferred as the first segment of a command.

21. (Previously Presented) The method of claim 16, further comprising:

generating, by the memory control device, coded commands; and

decoding the coded command at one or more of the plurality of memory modules.

22. (Cancelled)